What we claim is:

1. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein at least one pair of processors among said processors are positioned symmetrically relative to each other with respect to a given linear axis or a given origin in the plane of the chip.

2. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein at least one pair of processors among said processors are positioned symmetrically relative to each other with respect to a given linear axis or a given origin in the plane of the chip and the controller for said pair of processors is located in the area containing said linear axis or origin.

3. The on-chip multiprocessor as disclosed in claim 2, wherein delays between each processor of said pair and said controller are almost equal.

4. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein: at least one pair of processors among said processors are positioned symmetrically relative to each other with

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respect to a given linear axis or a given origin in the plane of the chip; delays in transmission between said multiprocessor controller and each processor of said pair of processors are almost equal; and the shared portions connected through the controller to said pair of processors are located in the area containing said linear axis or origin.

5. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein at least one pair of processors among said processors are situated at positions shifted from positions symmetric with respect to a given linear axis or a given origin in the plane of the chip, in a direction parallel to said axis or the centerline of the area of said pair.

6. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein: at least one pair of processors among said processors are situated at positions shifted from positions symmetric with respect to a given linear axis or a given origin in the plane of the chip, in a direction parallel to said axis or the centerline of the area of said pair; and the controller for said pair of processors is located in the area containing said linear axis or origin.

7. An on-chip multiprocessor wherein delays in transmission from each processor of said pair of processors to said controller are almost equal.

8. An on-chip multiprocessor having multiple independently operable processors mounted on an integrated circuit chip, wherein: at least one pair of processors among said processors are situated at positions shifted from positions symmetric with respect to a given linear axis or a given origin in the plane of the chip, in a direction parallel to said axis or the centerline of the area of said pair; delays in transmission between said controller and each processor of said pair of processors are almost equal; and the shared portions connected through said controller to said pair of processors are located in the area containing said linear axis or origin.

9. The on-chip multiprocessor as defined in claim 1, wherein said processors have logical units and cache memories, and in said pair of processors, two logical units or cache memories with the same function as a pair are symmetric relative to each other with respect to said linear axis or origin.

10. The on-chip multiprocessor as defined in claim 9,

wherein said logical units and cache memories have each logical blocks and memory mats, and in said pair of processors, two logical blocks or memory mats with the same function as a pair are symmetric relative to each other with respect to said linear axis or origin.

11. The on-chip multiprocessor as defined in claim 9, wherein said logical blocks and memory mats have each logical circuit groups and memory circuit groups, and in said pair of processors, two logical circuit groups or memory circuit groups with the same function as a pair are symmetric relative to each other with respect to said linear axis or origin.

12. The on-chip multiprocessor as defined in claim 9, wherein said logical circuit groups and memory circuit groups consist of MOS transistor circuits, and sources, gates and drains inside said circuit groups or p-MOS and n-MOS transistors are symmetric relative to each other with respect to said linear axis or origin.

13. The on-chip multiprocessor as defined in claim 12, wherein at least some of the MOS transistors in said pair of processors have one gate and a source and drain at one side of the gate, a drain and a source, opposite to said

source and drain, at the other side of the gate, and also have two gates through which a same signal is inputted, one drain between the gates, and two sources outside the gates.

14. The on-chip multiprocessor as defined in claim 1, wherein said processors comprise MOS transistor circuits, and said pair of processors are mirror-symmetric with respect to a linear axis parallel or perpendicular to the MOS transistor gate, or point-symmetric (180° rotation) with respect to said origin.

15. The on-chip multiprocessor as defined in claim 9, wherein said pair of processors are symmetric with respect to a linear axis parallel or perpendicular to the direction of data flow in said logical units, or point-symmetric (180° rotation) with respect to said origin.

16. An on-chip multiprocessor having multiple independently operable processors and their processor mounted on an integrated circuit chip, wherein: some of the logical units or cache memories constituting each processor are dual and redundant; in at least one pair of processors, two logical units or cache memories with the same function as a pair are symmetric relative to each other with respect to a given first linear axis in the chip plane; the controller for said pair of

processors is located in the area containing the first linear axis; the distances from said controller to both the processors are almost equal; and two logical units or cache memories as a dual unit included in each processor are symmetric relative to each other with respect to a given second linear axis.

17. The on-chip multiprocessor as defined in claim 16, wherein said first linear axis and second linear axis intersect at right angles.

18. The on-chip multiprocessor as defined in claim 16, wherein said processors comprise MOS transistor circuits, and said first linear axis is parallel to the MOS transistor gate width direction and said second linear axis is parallel to the MOS transistor gate length direction.

19. The on-chip multiprocessor as defined in claim 16, wherein said first linear axis is perpendicular to the direction of data flow in said logical units and said second linear axis is parallel to the direction of data flow.

20. The on-chip multiprocessor as defined in claim 2, wherein: said pair of processors also have cache memory shared by them, and storage control unit for controlling

processing of signals between said shared cache memory and said pair of processors; and said shared cache memory and storage control unit are located in said area.

21. The on-chip multiprocessor as defined in claim 2, wherein said pair of processors also share I/O circuit group, and storage control unit for controlling signal transmission between said I/O circuit group and said pair of processors is located in said area.

22. The on-chip multiprocessor as defined in claim 4, wherein a clock generator, which supplies clock signals in common or separately to said pair of processors, said controller and said shared portions, is located in said area.

23. The on-chip multiprocessor as defined in claim 4, wherein a power supply control circuit, which supplies electric power in common or separately to said pair of processors, said controller and said shared portions, is located in said area.

24. The on-chip multiprocessor as defined in claim 1, wherein: each of said processors has first cache memory and a first cache memory control unit for controlling it;

multiple processors share lower level cache memory through its control unit; in said pair of processors, the first cache control units are located beside one side of each processor area nearer to said linear axis or origin; and the lower level cache control unit is located between the first cache control units as a pair.

25. The on-chip multiprocessor as defined in claim 1, wherein: each of said processors has a first control unit for controlling its input/output signals; multiple processors share I/O circuit group through a second control unit; in said pair of processors, the first control units are located beside one side of each processor area nearer to said linear axis or origin; and the second control unit is located between the first control units as a pair.

26. The on-chip multiprocessor as defined in claim 1, wherein the pattern of clock trees which distribute clock signals to said pair of processors is symmetric with respect to said linear axis or origin.

27. The on-chip multiprocessor as defined in claim 1, wherein the pattern of power supply wiring which supplies electric power to said pair of processors is symmetric with respect to said linear axis or origin.

28. The on-chip multiprocessor as defined in claim 1, wherein the I/O pins of said processors consist of bump arrays and the arrangement of bumps on the surfaces of said pair of processors is symmetric with respect to said linear axis or origin.

29. The on-chip multiprocessor as defined in claim 1, wherein one processor in said pair of processors is manufactured using semiconductor mask pattern 1 and the other is manufactured using semiconductor mask pattern 2.

30. A circuit board wherein the on-chip multiprocessor as defined in claim 1 is mounted, wiring pattern 1 for one processor in said pair of processors and wiring pattern 2 for the other processor are symmetric each other with respect to a given linear axis on the circuit board or said origin.